IN THE CLAIMS

Please add new claims 23 - 24 as follows:

23. (NEW) A method of operating a semiconductor switching node, the semiconductor switch core comprising a semiconductor switch core and plural switch port devices, the semiconductor switch core comprising a buffer matrix having one buffer memory per crosspoint, plural switch core ports, the plural switch port devices being connected to corresponding ones of the plural switch core ports, the method comprising:

A2

in an appropriate one of the switch port devices, queuing in a queue for low priority cells a low priority cell awaiting writing to the corresponding crosspoint;

writing the low priority cell to the buffer memory for the corresponding crosspoint;

in the appropriate one of the switch port devices, queuing in a queue for high priority cells a high priority cell awaiting writing to the corresponding crosspoint;

providing an indication that the high priority cell awaiting writing to the corresponding crosspoint is in the queue for high priority cells;

reading out the low priority cell from the buffer memory for the corresponding crosspoint in response to the indication.

24. (NEW) The method of claim 23, further comprising writing the high priority cell to the buffer memory for the corresponding crosspoint after the low priority cell has been read out.